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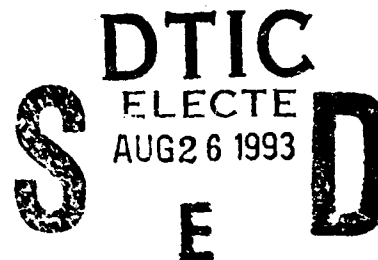
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August 9, 1993

Department of the Navy
Mr. Robert J. Silverman
ONR Resident Representative
University of Washington
410 University District Bldg.
1107 N.E. 45th Street
Seattle, Washington 98105-4631

Re: N00014-90-J-1793

Dear Mr. Silverman:

Enclosed please find a copy of the final report for the above-referenced grant which was submitted to program officer Dr. Clifford Lau on January 6, 1993. The purpose of this mailing is to ensure proper distribution of the report to all addressees as required by the grant document.

Should you have any additional questions or concerns regarding the close-out of this grant, please do not hesitate to call.

Sincerely,

Brenda L. Akins
Assistant Director

Enclosure

cc: Director, Naval Research Laboratory
Attn: Code 2627
Washington, DC 20375

Defense Technical Information Center
Building 5, Cameron Station
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S.M. Reddy (letter only)

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1. Objective

To insure correct operation of digital logic circuits one must ascertain that the circuits perform functionally correct operations, at desired speeds or clock rates. Extensive research has been expended to derive procedures to ascertain the correct functional behavior of logic circuits. For example, procedures to detect line stuck-at faults and other logic faults help identify faulty circuits that do not perform correct functional operations. Relatively much less effort has been expended to derive procedures to ascertain correct operations by digital logic circuit at desired clock rates. Circuit failures causing malfunctions while operating at desired clock rates, but may not at other clock rates, are modeled to test logic circuits to detect and locate delay faults and to develop methods to design logic circuits that are easily testable for delay faults.

2. Relevance to SDI

The computational and reliability requirements of SDI systems require the use of high throughput devices and systems of highest reliability. High throughput systems are derived by using high speed devices in large parallel and/or distributed computing configurations. To insure that systems operate at desired speeds, the constituent chips, subsystems and systems must be "checked out" at clock rates consistent with expected operational conditions. This implies, that reliable and cost effective methods be developed to test and ascertain correct functional operation, at operational clock rates, of digital logic circuits and systems. It is also important to develop methods to design digital systems such that their correct operation at desired speeds can be cost effectively ascertained. The objective of the research under this contract addresses these issues.

3. Summary of Research Performed

In this section research performed during the last three years of support is summarized. Correct operation of a logic circuit requires that the signal propagation delays along paths in the circuit be less than or more than a specified limit. Defects and/or random variations in process parameters often cause propagation delays to fall outside the desired limits. When the delay along a path falls outside the specified limit, a delay fault is said to have occurred. An often suggested method to detect delay faults is to apply an input vector V_1 to the circuit under test at time t_0 . After the signals in the circuit under test have stabilized, a second input vector V_2 is applied at time t_1 , such that a rising or falling transition is propagated from the input of the path under test, along the tested path, to the output of the path. By sampling the path output at time t_2 , where $(t_2 - t_1)$ corresponds to the desired operational time interval, one can ascertain the existence or nonexistence of a delay fault. In other words, to detect a path delay fault, a two-pattern test is applied that creates and propagates appropriate signal transitions along the path to be tested.

Delay faults causing propagation delays to be less than as well as more than specified limits are of concern. We have concentrated on faults causing larger than expected delays. However the methods developed are readily extendible to the problem of detecting delay faults leading to shorter than expected delays.

Two fault models have been proposed. One is the gate delay fault and the other is the path delay fault. Gate delay faults model those delay defects occurring at inputs or outputs of a gate, which cause the gate delay to be outside its specified range. Path delay faults model defects that cause cumulative propagation delays along circuit paths exceed the specified range. We are using both delay fault models.

We have investigated a class of tests called robust tests to detect path delay faults.

Definition 1: A two-pattern test $\langle V_1, V_2 \rangle$ is said to be robust delay test for path L_x if and only if, when L_x is faulty and test $\langle V_1, V_2 \rangle$ is applied, the circuit output is different from the expected state at sampling time t_2 , independent of the delays along gate input leads not on path L_x (note that the expected state at sampling time t_2 , independent of the output at time t_2 is the state of the path output corresponding to input V_2).

The importance of robust tests for delay faults can be seen by the following argument. Excessive delays in circuits under test are often due to device parameter variations caused by random fluctuations during fabrication of these circuits. Process variations affecting circuit delays could cause variations in delay characterizations of several devices in the circuit. Hence one must insure that tests to detect a path delay fault are not invalidated (masked) by delay characteristics of device not on the tested path. This is insured by the requirements imposed on robust tests defined above. These restrictions guarantee another important attribute of robust tests. Robust tests remain valid as long as the network does not change while technology or process changes.

We have also studied gate delay faults and a special case of gate delay faults called gross delay or transition faults. Gross delay faults are those faults that effect every path through the fault site such a way that the signal propagation along each path exceeds the clock interval. This assumption simplifies test generation and fault simulation.

Most of our research on delay faults has been for combinational logic circuits. During this time, we have also investigated several other topics related to testing of digital circuits, in order to identify deficiencies and propose methods to rectify such deficiencies, especially in the areas of sequential circuit testing and test data compaction. This effort was found necessary to continue our research.

3.1 Review of Accomplished Research Results

3.1.1 Path Delay Faults

Necessary and sufficient conditions for the existence of several classes of robust tests for circuit paths in combinational logic circuits were presented in [2]†. Methods to select a minimum set of paths in combinational logic circuits such that for each circuit lead r there are paths in the set such that the paths have maximum as well as minimum delay among all paths through r were presented in [8]. This allows testing of digital circuits for correct operation by selecting a minimum number of paths to verify compliance with timing specifications. Design of robustly testable combinational logic circuits were investigated in [11,17,29]. The methods always lead to 100% testable designs for combinational logic circuits. Methods to generate minimal size test sets to detect path delay faults in combinational logic circuits were investigated in [18]. Methods to generate tests in sequential logic circuits were investigated in [27]. This work reports the first method to test sequential circuits using system clock only, to detect delay faults. All other methods require varying system clock period, which is difficult and expensive to accommodate. A highly efficient and versatile fault simulator for path delay faults was developed [30]††. This work contains many results of potentially wider applications. For example it reports linear time algorithms to count paths in acyclic graphs and also reported is a method to label (selected) edges in acyclic graphs such that paths in the graph are associated with a unique integer index. This facilitates a highly efficient way to manage lists of paths in logic circuits. The method also included an efficient method to parallelize the computations that allowed simulation of large (10^{10}) input vectors in few hundred seconds on ISCAS-89 benchmark circuits using a workstation. An extremely efficient non-enumerative method to determine path delay fault coverage achieved by a given test sequence is reported in [33]. This is the first method available to determine fault coverage in extremely large circuits. For example circuits with 10^{16} paths were analyzed in less than 3 seconds of CPU time on a workstation. This non-enumerative method has now been extended to test generation for circuits with large number of testable paths. For the first time tests for 10^{16} paths were derived, compared to earlier methods that only considered tests for thousands of paths only [42]. The non-enumerative methods for determining fault coverage and test generation exposed the problem of deriving tests for circuits that require extremely large number of tests for some circuits. For example we showed that for a sixteen bit multiplier circuit, available as circuit c6288 in the ISCAS-85 benchmark suit, the number of tests to detect all path delay faults is over 10^{12} . In order to solve test generation

† References cited in this section are given in Section 3.2.

†† The paper reporting this work, [30], received the best paper award at EURO-DAC in September 1992.

problem for such circuits, in [42], we have investigated design for testability methods to derive circuits with reduced test set sizes.

3.1.2 Gate Delay Faults

Methods to test embedded self-checking checkers were investigated in [5]. A realistic fault model that captures expected process variations in VLSI chips called tracking delay fault model was proposed in [1]. It was shown how this model allows accurate estimation of fault coverage and the detection of chips that could malfunction due to delay defects. This is the only reported method that guarantees detection of all malfunctioning parts assuming gate delay faults model defects accurately. A definition of independent faults for transition faults was developed in [24]. Independent faults are those that cannot be detected by the same test and find use in establishing lower bounds on test set sizes. This was used in deriving short test sequences for FET stuck-open faults and transition faults in [32]. Transition faults model gross delay faults in logic circuits. A fault simulator for a class of gross delay faults in synchronous sequential circuits was reported in [25].

3.1.3 Synchronous Sequential Circuits

In order to extend our studies in delay fault testing, which until had concentrated on combinational logic circuits, to sequential logic circuits we initiated research into testing of synchronous sequential logic circuits. Even though the problem of generating tests for line stuck-at faults in synchronous sequential logic circuits has been studied for over 30 years, we found that the available methods suffer from several deficiencies. These deficiencies have caused the test generators to inaccurately label some detectable faults as undetectable and have caused loss of precision in handling unknown values of flip-flop states. Methods to make test generators for sequential circuits accurate were presented for the first time in [10,14,20]. Methods to accurately identify redundant stuck-at faults are proposed in [21, 51]. Several efficient methods to generate minimal test sequences for small to medium circuits are reported in [9,15]. A novel divide and conquer method to generate tests for large sequential circuits was reported in [28]. Other novel methods developed include the use of homing sequences to generate tests [57] which resulted in achieving 100% fault coverage for circuits for which earlier methods achieved very small ($< 1\%$) fault coverage and a method to use reset of only a subset of flip-flops (instead of the normally assumed good practice of resetting all flip-flops in a sequential circuit) to achieve high fault coverage.

3.1.4 Pseudo-random Testing and Aliasing

A cost effective way to generate tests, especially in built-in-self-test, environments is to use pseudo-random test vectors. Methods to reduce hardware costs for generating pseudo-random test vectors was reported in [22, 37, 47]. The method proposed uses only three weights instead of earlier proposals that used arbitrary number of weights to achieve high fault coverage. This reduced the cost of hardware to generate tests in built-in-self test environments. Responses of circuits and systems under test are often compressed to reduce test data in both off-line and in built-in-self-test environments. A problem with test data compaction is that it may lead to aliasing, causing loss of fault coverage. Several methods to achieve test data compaction with zero aliasing were reported in [23]. We also proposed a method to compute aliasing, exactly, using fault simulation with fault dropping [40]. This novel idea reduces simulation times compared to all earlier methods that required the use of fault simulation without fault dropping to compute aliasing exactly.

3.1.5 New Fault Models

We have investigated a new fault model called EXOP (for extended operation). Tests derived for this model have lead to higher coverage of defects expected in VLSI circuits and systems [50]. Simulations indicate that tests for EXOP faults cover all stuck-open faults, transition faults, line stuck-at faults, and a very high percentage of bridging faults.

3.1.6 Fault Location

Much of the research we and other researchers in testing, have done has been to develop methods to detect faults. Fault diagnosis or fault location has received very little attention. We have initiated this research and developed methods to derive extremely small dictionaries for use in locating defects [34, 56]. We have also shown that contrary to earlier notion that dictionary based fault location strategies are always more expensive (in computer time and storage requirements) than dynamic fault location, dictionary based diagnosis is actually better under some practical circumstances. The conditions under which this is true were analytically studied.

3.1.7 Scalable Approaches to Test Generation and Design

Current research in testing and design emphasizes study of methods to apply to solve given specific problem. Heuristics are used to hold the cost of computation reasonable. However these approaches lack inherent ability to scale to larger problems, typically resulting in either high computational demands or low solution quality. We have investigated a new and scalable approach to solve problems in testing and design. The method uses dynamic learning on problems of small size to solve problems of larger size. Initial results on test generation are reported in [43].

3.2 Publications During 1990-92

- [1] Pramanick, A.K. and Reddy, S.M., "On the Fault Coverage of Delay Fault Detection Tests," Proc. European Design Automation Conference, March 1990, pp. 334-367.
- [2] Pramanick, A.K. and Reddy, S.M., "On the Design of Path Delay Fault Testable Combinational Circuits," Proc. Int. Symp. on Fault-tolerant Computing, June 1990, pp. 374-381.
- [3] Gupta, S.K., Pradhan, D.K. and Reddy, S.M., "Zero Aliasing Compression," Proc. Int. Symp. on Fault-tolerant Computing, June 1990, pp. 254-263.
- [4] Kundu, S. and Reddy, S.M., "On Symmetric Error Correcting and All Undirectional Error Detecting Codes," IEEE Trans. Comp., June 1990, pp. 752-761.
- [5] Kundu, S. and Reddy, S.M., "Embedded Totally Self-checking Checkers: A Practical Approach," IEEE Design and Test, August 1990, pp. 5-12.
- [6] Kundu, S. and Reddy, S.M., "Robust Tests for Parity Trees," Journal of Electronic Circuit Testing: Theory and Applications, October 1990, pp. 191-200.
- [7] Lee, D.H. and Reddy, S.M., "On Determining Scan Flip-Flops in Partial-Scan Designs," Proc. ICCAD, November 1990, pp. 322-325.
- [8] Li, W.N., Reddy, S.M., and Sahni, S., "Long and Short Covering Edges in Combinational Logic Circuits," IEEE T-CAD, December 1990, pp. 1245-1253.
- [9] Pomeranz, I. and Reddy, S.M., "On Achieving a Complete Fault Coverage for Sequential Machines Using the Transition Fault Model," 28th Design Automation Conference, June 1991, pp. 341-346.
- [10] Pomeranz, I. and Reddy, S.M., "Test Generation for Synchronous Sequential Circuits Using Multiple Observation Times," 21st Fault-Tolerant Computing Symposium, June 1991, pp. 52-59.
- [11] Kundu, S., Reddy, S.M., and Jha, N.K., "Design of Robustly Testable Combinational Logic Circuits," IEEE Trans. on CAD, August 1991, pp. 1036-1048.
- [12] Pomeranz, I. and Reddy, S.M., "Testing of Fault-Tolerant Hardware," 5th Intl. Conference on Fault-Tolerant Computing Systems, pp. 148-159, September 1991.
- [13] Lee, D.H. and Reddy, S.M., "A New Test Generation Method for Sequential Circuits," Proc. ICCAD, November 1991, pp. 446-449.
- [14] Pomeranz, I., Reddy, S.M. and Reddy, L.N., "Increasing Fault Coverage for Synchronous Sequential Circuits by the Multiple Observation Time Test Strategy," Intl. Conference on Computer-Aided Design, November 1991, pp. 454-457.
- [15] Pomeranz, I. and Reddy, S.M., "Test Generation for Synchronous Sequential Circuits Based on Fault Extraction," Intl. Conference on Computer-Aided Design, November 1991, pp. 450-453.
- [16] Pomeranz, I., Reddy, L.N. and Reddy, S.M., "COMPACTEST: A Method to Generate Compact Test Sets for Combinational Circuits," Intl. Test Conference, 1991, pp. 194-203.
- [17] Pomeranz, I. and Reddy, S.M., "Achieving Complete Delay Fault Testability by Extra Inputs," Intl. Test Conference, 1991, pp. 273-282.
- [18] Pramanick, A.K. and Reddy, S.M., "On Multiple Path Propagating Tests for Path Delay Panels," Intl. Test Conference, 1991, pp. 393-402.
- [19] Pomeranz, I. and Reddy, S.M., "3-Weight Pseudo-Random Test Generation Based on a Deterministic Test Sets," VLSI Design Conference, January 1992.
- [20] Pomeranz, I. and Reddy, S.M., "The Multiple Observation Time Test Strategy," IEEE Transactions on Computers, May 1992 (special issue on Fault-Tolerant Computing), pp. 627-637.

- [21] Pomeranz, I. and Reddy, S.M., "Classification of Faults in Synchronous Sequential Circuits," to appear in the IEEE Transactions on Computers, also available as Technical Report No. 3-27-1991, Electrical and Computer Engineering Department, University of Iowa.
- [22] Pomeranz, I. and Reddy, S.M., "3-Weight Pseudo-Random Test Generation Based on a Deterministic Test Set," 1992 VLSI Design Conference, Jan. 1992, pp. 148-153.
- [23] Pomeranz, I., Reddy, S.M. and Tangirala, R., "On Achieving Zero Aliasing for Modeled Faults," European Conference on Design Automation, March 1992, pp. 291-299.
- [24] Pomeranz, I. and Reddy, S.M., "Generalization of Independent Faults for Transition Faults," in Proc. VLSI Test Symposium, Atlantic City, April 1992, pp. 7-12.
- [25] Lee, D.H. and Reddy, S.M., "On Efficient Concurrent Fault Simulation for Synchronous Sequential Circuits," Proc. 29th Design Automation Conference, June 1992, pp. 327-331.
- [26] Reddy, L.N., Pomeranz, I. and Reddy, S.M., "ROTCO: A Reverse Order Test Compaction Technique," Proc. EURO-ASIC '92, June 1992, pp. 189-194.
- [27] Pomeranz, I. and Reddy, S.M., "At-Speed Delay Testing of Synchronous Sequential Circuits," 29th Design Automation Conference, June 1992, pp. 177-181.
- [28] Pomeranz, I. and Reddy, S.M., "A Divide-and-Conquer Approach to Test Generation for Large Synchronous Sequential Circuits," 22nd International Fault-Tolerant Computing Symposium, July 1992, pp. 230-237.
- [29] Jha, N.K., Pomeranz, I., Reddy, S.M. and Miller, R.J., "Synthesis of Multi-Level Combinational Circuits for Complete Robust Path Delay Fault Testability," 22nd International Fault-Tolerant Computing Symposium, July 1992, pp. 280-287.
- [30] Pomeranz, I., Reddy, L.N. and Reddy, S.M., "SPADES: A Simulator for Path Delay Faults in Sequential Circuits," EURO-DAC'92, September 1992, pp. 428-435.
- [31] Pomeranz, I. and Reddy, S.M., "A Test Application Scheme for Embedded Full-Scan Circuits to Reduce Testing Costs," Asia Test Symp., November 1992.
- [32] Reddy, L.N., Pomeranz, I. and Reddy, S.M., "COMPACTEST-II: A Method to Generate Compact Two-Pattern Test Sets for Combinational Logic Circuits," Proc. ICCAD'92, November 1992, pp. 568-574.
- [33] Pomeranz, I. and Reddy, S.M., "An Efficient Non-Enumerative Method to Estimate Path Delay Fault Coverage," Proc. ICCAD'92, November 1992, pp. 560-567.
- [34] Pomeranz, I. and Reddy, S.M., "On the Generation of Small Dictionaries for Fault Location," Proc. ICCAD'92, November 1992 pp. 272-279.
- [35] Shrivastava, Y., Dasgupta, S., and Reddy, S.M., "Guaranteed Convergence in a Class of Hopfield Networks," IEEE Trans. on Neural Networks, November 1992, pp. 951-962.
- [36] Paik, D., Reddy, S.M., and Sahni, S., "Heuristics for the Placement of Flip-flops in Partial Scan Designs and the placement of Signal Boosters in Lossy Circuits," VLSI-Design '93, January 1993, pp. 45-50.
- [37] Pomeranz, I. and Reddy, S.M., "On the Generation of Weights for Weighted Pseudo Random Testing," VLSI Design '93, January 1993, pp. 69-72.
- [38] Pramanick, A. and Reddy, S.M., "On Unified Delay Fault Testing," VLSI Design '93, January 1993, pp. 265-268.
- [39] Shahookar, K., Khamisani, W., Mazumder, P., and Reddy, S.M., "Genetic Beam Search for Gate Matrix Layout," VLSI Design '93, January 1993, pp. 208-213.
- [40] Pomeranz, I. and Reddy, S.M., "Aliasing Computation Using Fault Simulation with Fault Dropping," VLSI Test Symposium, April 1993.
- [41] Pomeranz, I. and Reddy, S.M., "Fault Simulation for Synchronous Sequential Circuits Under the Multiple Observation Time Testing Approach," European Test Conference, April 1993.

- [42] Pomeranz, I., Reddy, S.M., and Uppaluri, P., "NEST: A Non-enumerative Test Generation Method for Path Delay Faults in Combinational Circuits," Design Automation Conference, June 1993.
- [43] Pomeranz, I. and Reddy, S.M., "INCREDIBLE-TG: INCREmental DYnamic Test Generation Based on LEarning," Design Automation Conference, June 1993.
- [44] Pomeranz, I. and Reddy, S.M., "On Achieving Complete Fault Coverage for Sequential Machines," accepted for IEEE Transactions on Computer Aided Design.
- [45] Pomeranz, I. and Reddy, S.M., "On the Role of Hardware Reset in Synchronous Sequential Circuit Test Generation," accepted for IEEE Transactions on Computers.
- [46] Pomeranz, I. and Reddy, S.M., "Testing of Fault-Tolerant Hardware Through Partial Control of Inputs," accepted for IEEE Transactions on Computers.
- [47] Pomeranz, I. and Reddy, S.M., "3-Weight Pseudo-Random Test Generation Based on a Deterministic Test Set," accepted for IEEE Transactions on Computer Aided Design.
- [48] Pomeranz, I. and Reddy, L.N., and Reddy, S.M., "COM (FTCS-93)PACTEST: A Method to Generate Compact Test Sets for Combinational Circuits," accepted for IEEE Transactions on Computer Aided Design.

Papers Under Review

- [49] Pomeranz, I. and Reddy, S.M., "Design and Synthesis for Testability of Synchronous Sequential Circuits Based on Strong-Connectivity," Submitted to International Symposium on Fault-Tolerant computing.
- [50] Pomeranz, I. and Reddy, S.M., "EXOP (Extended Operation): A New Logical Fault Model for Digital Circuits," submitted to FTCS-93.
- [51] Patel, J.H., Pomeranz, I., and Reddy, S.M., "Theory and Practice of Sequential Machine Testing and Testability," submitted to FTCS-93.
- [52] Kajihara, S., Pomeranz, I., Kinoshita, K., and Reddy, S.M., "Cost-effective Generation of Minimal Test Sets for Stuck-at Faults in Combinational Logic Circuits," submitted to DAC-93.
- [53] Pomeranz, I. and Reddy, S.M., "Generalization of Independent Faults Requiring Two-Pattern Test," submitted to The Journal of Electronic Testing: Theory and Applications.
- [54] Pomeranz, I. and Reddy, S.M., "SPADES-ACE: A Simulator for Path Delay Faults in Sequential Circuits with Extensions to Arbitrary Clocking Schemes," submitted to IEEE Transactions on CAD.
- [55] Pomeranz, I. and Reddy, S.M., "An Efficient Non-Enumerative Method to Estimate the Path Delay Fault Coverage in Combinational Circuits," submitted to IEEE Transaction on CAD.
- [56] Pomeranz, I. and Reddy, S.M., "On Dictionary Based Fault Location in Digital Logic Circuits," submitted to IEEE Transactions on CAD.
- [57] Pomeranz, I. and Reddy, S.M., "Application of Homing Sequences for Synchronous Sequential Circuits," submitted to IEEE Transactions on Computers.
- [58] Pomeranz, I. and Reddy, S.M., "On the Number of Tests to Detect All Path Delay Faults in Combinational Logic Circuits," submitted to IEEE Transactions on Computers.
- [59] Shrivastava, Y., Dasgupta, S., and Reddy, S.M., "Non-positive Hopfield Networks for Unidirectional Error Correcting Coding," submitted to IEEE Transactions on Circuits and Systems.

3.3 Graduate Theses During 1990-92

- (1) A.K. Pramanick, "Testing and Design for Testability for Delay Faults in Combinational Logic Circuits," Ph.D. Thesis, Department of Electrical and Computer Engineering, University of Iowa, Iowa City, Iowa, August 1991.
- (2) M.K. Reddy, "Testable Digital CMOS Designs and Switch-Level Test Generation for MOS Digital Circuits," Ph.D. Thesis, Department of Electrical and Computer Engineering, University of Iowa, Iowa City, Iowa, August 1992.
- (3) R. Jain, "On Codeword Testing of 2-Rail and Parity Code Self-Checking Checkers," M.S. Thesis, Department of Electrical and Computer Engineering, University of Iowa, Iowa City, Iowa, May 1992.
- (4) D.H. Lee, "Test Generation and Partial Scan Design for Synchronous Sequential Circuits," Ph.D. Thesis, Department of Computer Science, University of Iowa, Iowa City, Iowa, August 1992.
- (5) L.N. Reddy, "Compact Test Sets for Digital Logic Circuits," Ph.D. Thesis, Department of Electrical and Computer Engineering, University of Iowa, Iowa City, Iowa, August 1992.

3.4 Awards and Honors

Best Paper Award, Euro-DAC, September 1992, "SPADES: A Simulator for Path Delay Faults in Sequential Circuits," Proc. Euro-DAC, pp. 428-435.

3.5 Names of Student Participants

J. Antes
H. Gatti
A.K. Gunda
R. Jain
D.H. Lee
A.K. Pramanick
L.N. Reddy
M.K. Reddy
B. Schulz
S. Sengupta
S. Seth
R. Tangirala
P. Uppaluri
S. Yadavalli